Application No.: 10/643,164   Docket No.: 102323-0130

REMARKS

Claims 47-57 stand rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,792,441 of Jaber. As discussed during the Telephone Interview on March 29, 2005, not only is that patent **not** prior art, it fails to teach or suggest the claimed invention.

Interview Summary

Applicant's undersigned representative discussed the subject application with the Examiner on March 29, 2005. The undersigned emphasized, as discussed in the **Amendment After Final Action** filed February 28, 2005, that Jaber was not prior art. The Examiner suggested that an affidavit would be necessary to support this. Although applicant can supply that affidavit, the late stage of prosecution would seem to preclude its presentation. Hence, as suggested at Interview, the Applicant shows below that Jaber fails to teach or suggest the claimed invention in the first instance.

Jaber is Not Prior Art

As discussed in Applicant's prior response, that patent is not prior art relative to the present application. Applicant's argument in this regard is incorporated herein by reference.

Jaber Fails to Teach or Suggest the Claimed Invention

Applicant's independent claim 47 is directed to a system for performing a fast Fourier transform on N ordered inputs in n stages comprising a non-final stage calculating means for repetitively performing in-place butterfly calculations for n-1 stages, and a final stage calculating means for performing a final stage of butterfly calculations. The final stage includes a first loop means and a second loop means. The first loop means performs a portion of the final stage butterfly calculations, by performing a set of butterfly calculations and storing the outputs in shuffled order in place of the selected inputs to result in a correct ordering of transform outputs. The second loop means performs the remaining portion of the final stage butterfly calculations, by performing two sets of butterfly calculations. The outputs from the first of the two sets are stored in shuffled order in place of the inputs selected for the second of the two sets of butterfly

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calculations. The outputs from the second of the two sets is stored in shuffled order in place of the inputs selected for the first one of the two sets of butterfly calculations to result in a correct ordering of transform outputs.

Jaber purports to teach the computation of a discrete Fourier transform (DFT) by calculating partial DFTs using a plurality of separate parallel processors, the outputs from which are combined in a single stage of butterfly calculations. The disclosure touts a configuration that said to decrease the burden of communications between the parallel processors, each of which performs computations independently, and the outputs of which are not combined until a final stage.

Jaber is in the category of inventions that this application sought to improve. Jaber assumes the bits are reversed before the start of the butterfly calculations (for example, see col. 12, lines 22-45) in order to produce output bits that are in the correct order. This is a classic example of prior art that requires pre- or post-processing of the bits to achieve the correct bit order (see below). This is the very thing the patentees were seeking to improve upon by reordering the bits during the butterfly calculations. Thus, referring to specification as filed, at page 3, lines 14-20, the applicant states:

> The order of the inputs to, and outputs from, an FFT calculation is important because typical FFT algorithms result in the outputs being in "bit-reversed" order from the inputs. While algorithms for reordering the outputs to be in natural order (or reordering the inputs to be in bit reversed order) are known in the art, additional processing steps must be employed to perform the reordering. Because FFTs are often calculated many at a time, processing time could be meaningfully reduced if an improved ordering scheme could be applied.

Turning now to the claims, nowhere does Jaber teach or suggest shuffling the order of the bits during the butterfly calculation stages as in the independent claim of the application (see claim 47, clauses 3 and 4, requiring shuffling the bit order during the first and second loop means of the final stage of butterfly calculations). Instead, Jaber shuffles the bits before the butterfly calculations in a completely separate process independent from the butterfly calculations. Specifically, Jaber uses an algorithm to create bit-reversed *inputs* to the processors. See Jaber at col. 12, lines 22-45. As with the prior art which the claimed invention supercedes, it is necessary that Jaber do this in order to provide correctly arranged outputs.

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To repeat the point, Jaber's shuffling the bit order is not performed as part of a butterfly stage -- as required by the claimed invention -- but rather is the result of a *pre-processing algorithm* done prior to the butterfly stages. For example, Jaber's Figures 1B and 10-11, which are referenced by the Examiner in Paragraph 7 of the Final Office Action, all show the processors with shuffled bits as *inputs*. Thus, again, contrary to the claimed invention, Jaber does not suffle bit order as part of a butterfly stage, but rather does so before even beginning the butterfly calculations.

In the claimed invention, to the contrary, the bit order is shuffled during the final stage of butterfly calculations by using two loop means for performing this final stage. Utilizing this system, embodiments of applicant's claimed invention accept correctly ordered bits as input and produce correctly ordered bits as outputs, with the reordering occurring within the butterflies. This has the advantage of speeding processing since, for example, the bit-reversing preprocessing stages of Jaber (and the corresponding post-processing stages of other prior art systems) are avoided.

Thus, in addition to the fact that it is not prior art, Jaber fails to teach or suggest the invention of claim 47. Claims 48-51 are dependent on independent claim 47, and contain all the features of claim 47. Hence, claims 48-51 are also patentable over Jaber.

The above arguments apply with equal force to independent claims 52 and 55, which parallel claim 47 in relevant regards, and all of their dependent claims. Hence, claims 52-57 are also patentable over Jaber.

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Conclusion

In view of the above, the pending application is in condition for allowance.

Dated: 4/29/05   Respectfully submitted,

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